LZ95F50

Timing Pulse Generator LSI for CCD

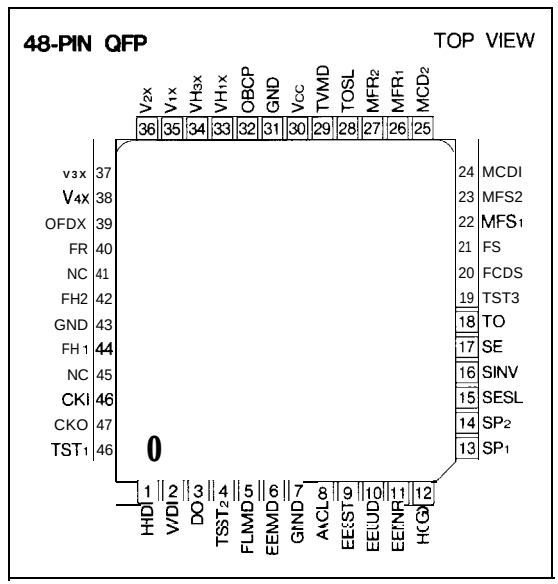
DESCRIPTION

The LZ95F50 is a CMOS timing generator LSI which provides timing pulses used to drive a CCD area sensor, in combination with the SSG LSI (LZ93N 19, LZ93B53).

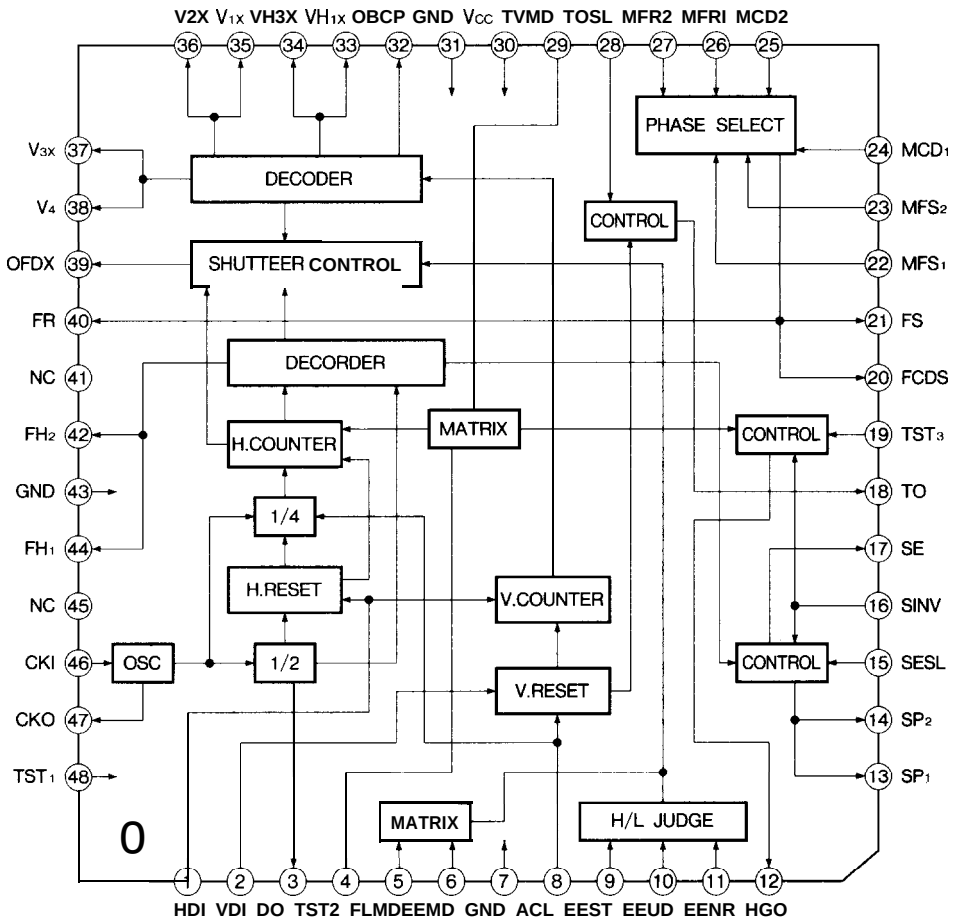
FEATURES

- Switchable **between 270000 pixels CCD and 320000 pixels CCD**
- Switchable **between NTSC** (EIA) **and PAL** (CCIR) **systems**
- **Built-in EE (Electronic Exposure) control**
- **Flicker-less function**
- **Single +5 V power supply**
- **Package : 48-pin QFP(QFP048-P-101 O)**

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to + 7.0	V
Input voltage	V_I	− 0.3 to V_{CC} + 0.3	V
Output voltage	V_O	− 0.3 to V_{CC} + 0.3	V
Operation temperature	Topr	−30 to +75	°C
Storage temperature	Tstg	−55 to +150	°C

DC CHARACTERISTICS

(V_{CC} = +5 V ± 10%, Ta = −30 to +75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Low level Input voltage	V_{IL}				1.5	V	1
High level Input voltage	V_{IH}		3.5			V	
Low level Input voltage	V_{T-}		1.0			V	2
High level Input voltage	V_{T+}				3.7	V	
Hysteresis voltage	$V_{T+} - V_{T-}$		0.4			V	
Low level Input current	$\lvert I_{IL1} \rvert$	V_I = 0 V			1.0	μA	3
	$\lvert I_{IL2} \rvert$	V_I = 0 V	6.0		75	μA	4
High level Input current	$\lvert I_{IH1} \rvert$	V_I = V_{CC}			1.0	μA	5
	$\lvert I_{IH2} \rvert$	V_I = V_{CC}	6.0		75	μA	6
Low level output voltage	V_{OL1}	I_{OH} = 3.2 mA			0.4	V	7
High level output voltage	V_{OH1}	I_{OL} = − 1.6 mA	4.0			V	
Low level output voltage	V_{OL2}	I_{OH} = 9.6 mA			0.4	V	8
High level output voltage	V_{OH2}	I_{OL} = −4.8 mA	4.0			V	

NOTES :

1. Applied to inputs (IC, ICD, ICU, ICK)
2. Applied to input (ICS).
3. Applied to inputs (IC, ICD, ICK).
4. Applied to input (ICU).
5. Applied to inputs (IC, ICD, ICK).
6. Applied to input (ICD).
7. Applied to outputs (O, OR1, OCK).
8. Applied to output (OR1 3).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	HDI	IC	IL	Horizontal draive pulse	A pin to input the horizontal reference pulse. To be connected to the HD pin of SSG-LSI.
2	VDI	ICS	⎍	Vertical drive pulse	A pin to input the vertical reference pulse. To be connected to the VD pin of SSG-LSI.
3	DO	o	⎍⎍	Delay-line clink	A pin to output 1/2 dividing pulse of CKI (pin 46). To be connected to the clock-input pin of SSG LSI. At NTSC mode : 606 fH At PAL mode : 618 fH (fH = Horizontal frequency)
4	TST2	ICU	–	CCD select input	An input pin to select the CCD type. L : A-type CCD H : B-type CCD
5	FLMD	ICU	–	Shutter speed select	An input pin to select the Flicker-less Shutter mode. For details, see "NOTES 2, 3".
6	EEMD	ICU	–	EE control 1	An input pin to select the EE Shutter Control mode. For details, see "NOTES 2, 3".
7	GND	–	–	Ground	A grounding pin. To be connected to the GND level.
8	ACL	ICU	⎍	Reset pulse	An input pin to reset at power ON. For details, see "NOTE 1 "
9	EEST	Icu	–	EE control enable	An input pin to enable the EE control. L : Make to stop the EE control. H : Make to start the EE control.
10	EEUD	IC	–	EE control 2	An input pin to control the up/down of shutter speed. For details, see "NOTE 3".
11	EENR	IC	–	EE control 3	
12	HGO	o	⎍⎍	Line switch output	A pulse to use in color separator. The signal switches between H and L at every line. The switching condition is selected by TST3 (pin 19).
13	SP1	0	⎍	Sampling pilse 1	A pin to output the sampling pulse for color demoduration based upon the output signal of CCD. It outputs at High level of the SE (pin 17).
14	SP2	0	⎍	Sampling pulse 2	A pin to output the sampling pulse for color demduration based upon the output signal of CCD. It outputs at Low level of the SE (pin 17).
15	SESL	ICU	–	SP1 and SP2 control	An input pin to select color demodulation carrier phase,
16	SINV	ICU	–	Carrier invert	An input pin to invert color demodulation carrier every horizontal pulse.

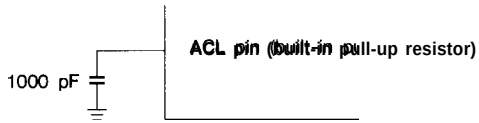
PIN NO.	SYMBOL	I/O	POLABITY	PIN NAME	FUNCTION
17	SE	o	⊓⊔⊓	Color demodulation pulse	A pin to output the color demodulation carrier.
18	TO	**0**	⊓	Control pulse	A pin to output calling pulse.
19	TST3	Icu	–	**HGO polarity control**	**An input pin to select the condition of** HGO (pin 12) output, L : Output direct to HGO (pin 12) the pulse **which is input** to SINV (pin 16), H : Output to HGO (pin 12) the signal which **invert the input to** SINV (pin 16) at PAL mode.
20	FCDS	OR1	⊔	CDS pulse	A pulse to clamp the signals from CCD. For details, sea "NOTE 4"
21	FS	ORI	⊔	Sample-hold pulse	A pulse to sample-hold the signals from CCD. For details, see "NOTE 4".
22	MFSI	Icu	–	FS phase control 1	**An input pin to control the phase of FS (pin** 21) output. For details, see "NOTE 4".
23	MFS2	ICU	-	FS phase control 2	
24	MCD 1	ICU	–	'CDS phase control 1	An input pin to control the phase of FCDS (pin 20) output. For details, see "NOTE 4".
25	MCD2	ICU	–	FCDS phase control 2	
26	MFRI	ICU	–	FR phase control 1	An input pin to control the phase of FR (pin 40) output. For details, see "NOTE 4".
27	MFR2	ICU	–	FR phase control 2	
28	TOSL	ICU	-	TO control	An input pin to control the TO (pin 18) output. L : TO output is stopped H : Output 10 pulses **to TO (pin** 18) after TOSL rise.
29	TVMD	ICD	–	TV mode select	**An input pin to select TV standard.** **L : NTSC mode H : PAL mode**
30	Vcc	–	–	**Power supply**	**To be connected to +5 V** power.
31	**GND**	**-**	**-**	**Ground**	**A grcunding pin. To be connected to the GND level.**
32	**OBCP**	o	⊔	**OB clamp**	**A pulse to clamp the optical black signals.**
33	**V Hix**	o	⊓	**Read out pulse 1**	**An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 1 BX pin of the LR38883N vertical driver LSI.**
34	**VH3X**	o	⊓	**Read out pulse 3**	**An output pin to transfer the photodiode charge of CCD to the vertical shift register. To be connected to the 3BX pin of the LR36883N vertical driver LSI.**

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
35	VI x	O		Vertical transfer pulse 1	Vertical transfer pulse. To be connected to the 1 AX pin of the LR36663N vertical driver LSI.
36	V2X	O		Vertical transfer pulse 2	Vertical transfer pulse. To be connected to the 2AX pin of the LR36663N vertical driver LSI.
37	V3X	o		Vertical transfer pulse 3	Vertical transfer pulse, To be connected to the 2AX pin of the LR36663N vertical driver LSI.
38	V4X	0		Vertical transfer pulse 4	Vertical transfer pulse. To be connected to the 2AX pin of the LR36663N vertical driver LSI.
39	OFDX	0		OFD pulse output	An output pin to sweep the photodiode charge of CCD. When FLMD and EEMD are Low level, this output becomes High level.
40	FR	0R13		Reset pulse	An output pin to reset the CCD output signals. To be connected to ϕ_{RS} pin of the CCD through the DC offset circuit. For details, sea "NOTE 4".
41	NC	–	–	No connection	No connected pin. A pin for no use.
42	FH2	OR13		Horizontal transfer pulse 2	Horizontal transfer pulse. To be connected to ϕ_{H2} pin of the CCD area sensor.
43	GND	–	–	Ground	A grounding pin. To be connected to the GND level.
44	FH 1	0R13		Horizontal transfer pulse 1	Horizontal transfer pulse. To be connected to ϕ_{H1} pin of the CCD area sensor.
45	NC	–	--	No connection	No connected pin. A pin for no use.
46	CKI	ICK	MM	Clock input	A pin for oscillation inverter input. NTSC : 19.069928 MHz (1212 fH) PAL : 19.3125 MHz (1236 fH) (fH = Horizontal frequency)
47	CKO	OCK		Clock output	A pin for oscillation inverter output.
48	TSTI	ICU	–	Test terminal	Testting pin. typically connected to the GND level.

IC Input pin (CMOS level).
ICD Input pin (CMOS level with built-in pull-down resistor)
ICU Input pin (CMOS level with built-in pull-up resistor).
ICS Input pin (CMOS level schmitt buffer).
o Output pin.
ORI, 0R13 Output pin (Through rate controlled buffer).
ICK Input pin for oscillation.
OCK Output pin for oscillation.

NOTES :

1. **How to use ACL pin (Pin 8)**



2. Fixad Shutter mode

EEMD (Pin 6)= Low level

FLMD (Pin 5)	SHUTTER SPEED (S)	
	NTSC	PAL
L	1 /60	1 /50
H	1/1 00 (Flicker-leas)	

3. EE CONTROL MODE

EEMD (Pin 6)= High level

FLMD (Pin 5)	SHUTTER SPEED (s)	
	NTSC	PAL
	1/61-1/50 000	1/51-1/50 000

EEUD	EENR	
	L	Shutter speed up
H		
		Control stopped
	H	
L		Shutter speed down

- **When EENR and EEUD are H level, control is stopped.**
- **When either EENR or EEUD is L level, control is resumed.**
- **When EEST set to L level, EE control is dieable.**

The shutter speed changes in the table es shown below

SHUTTER SPEED (s)	NTSC	1/61 to 1/230	to 1 /775	to 1/4 756	to 1/51 263
	PAL	1/51 m 1/222	to 1 /701	to 1/4 733	to 1/51 915
CHANGE STEP (S)	NTSC	1/1 750	1/3 930	1/15734	1 /63 000
	PAL	1/1 740	1/5210	1/15 625	1 /50 600

4. The phase adjustments should be made with the input combinations as shown in the table.

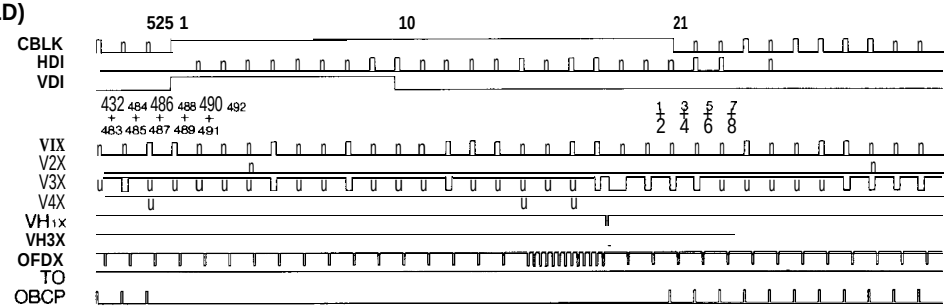
FR PHASE		FCD8 PHA8E		FS PHASE		PHASE DELAY (ns)
MFR_1	MFR2	MCD_1	MCD_2	MFS_1	MFS_2	
L	L	L	L	L	L	td
L	H	L	H	L	H	$td+\alpha$
H	L	H	L	H	L	$td+2\alpha$
H	H	H	H	H	H	$td+3\alpha$

TIMING DIAGRAM

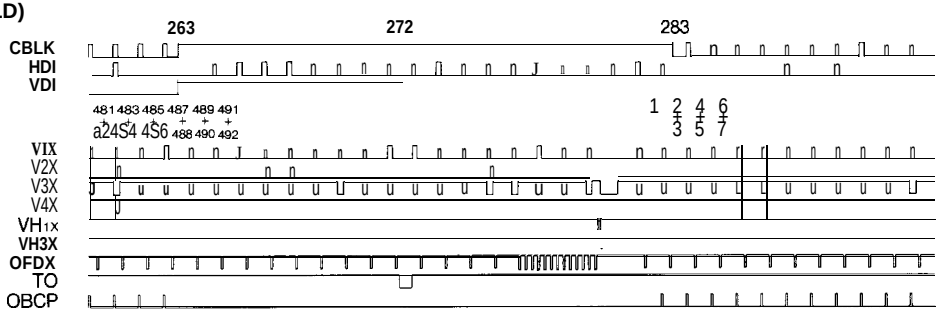
Shutter speed 1/50000 s

VERTICAL PULSE TIMING < NTSC >

(ODD FIELD)



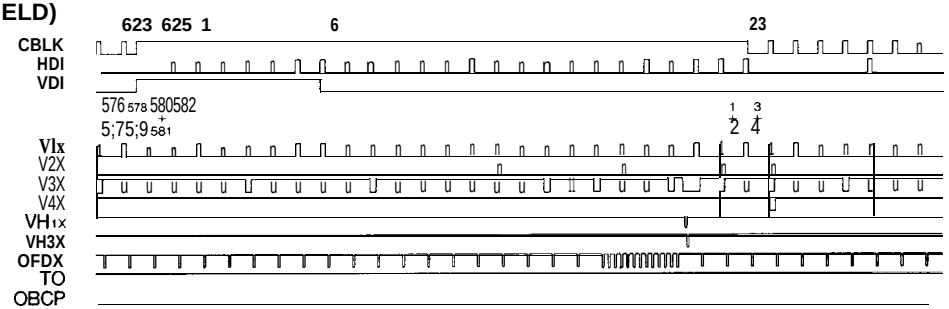
(EVEN FIELD)



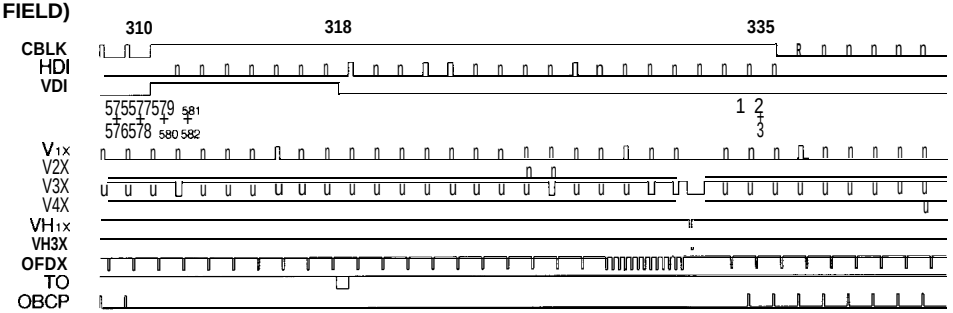
Shutter speed 1/50000 s

VERTICAL PULSE TIMING < PAL >

(1st, 3rd FIELD)

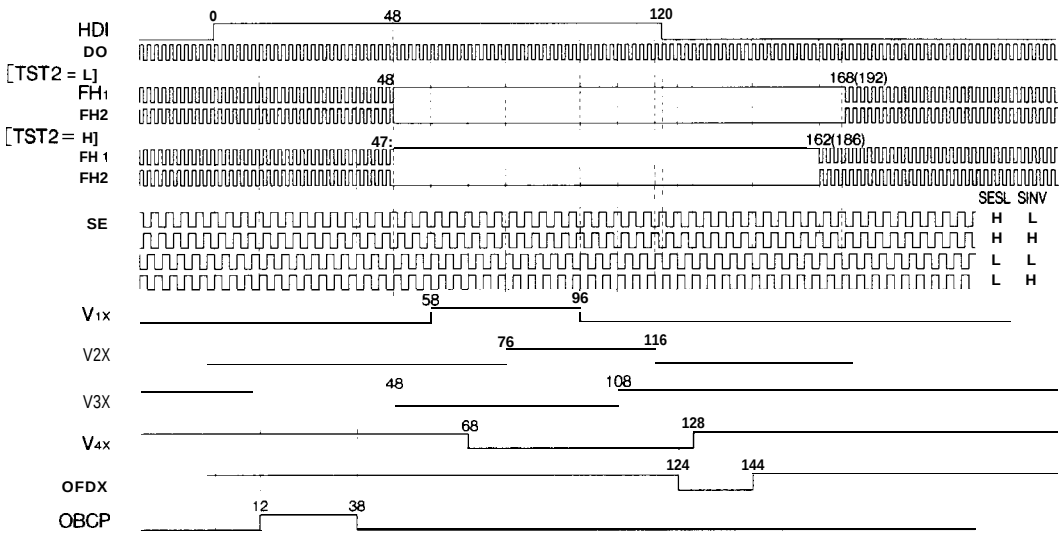


(2nd, 4th FIELD)



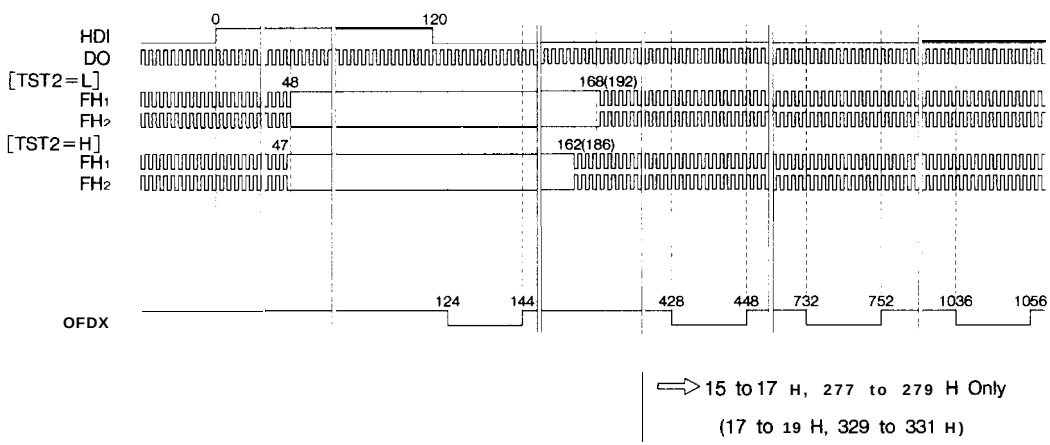
HORIZONTAL PULSE TIMING

( ) =PAL



"OFDX" PULSE TIMING

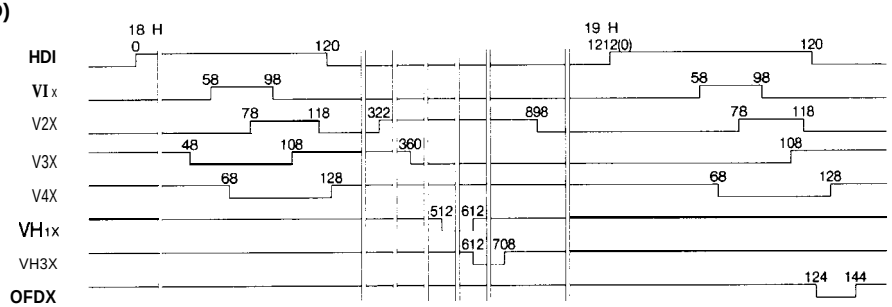
( ) =PAL



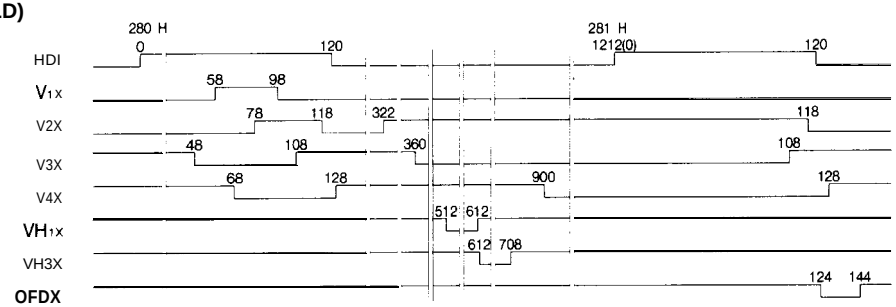
⇨ 15 to 17 H, 277 to 279 H Only
(17 to 19 H, 329 to 331 H)

CHARGE READ TIMING < NTSC >

(ODD FIELD)

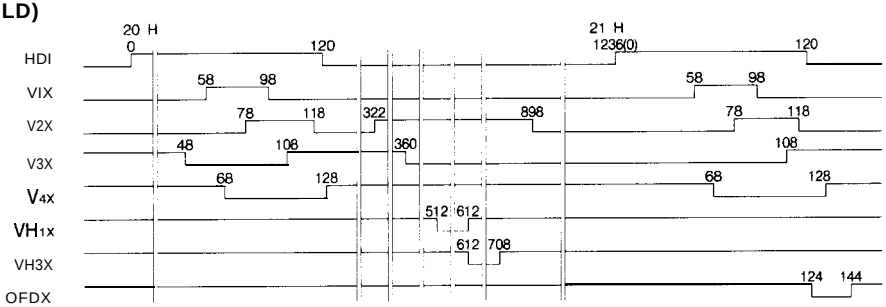


(EVEN FIELD)

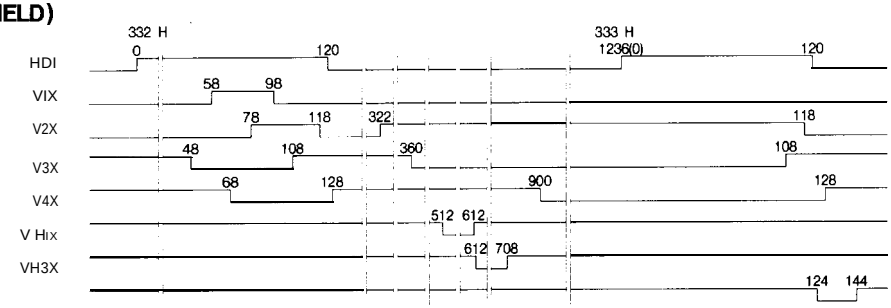


CHARGE READ TIMING < PAL >

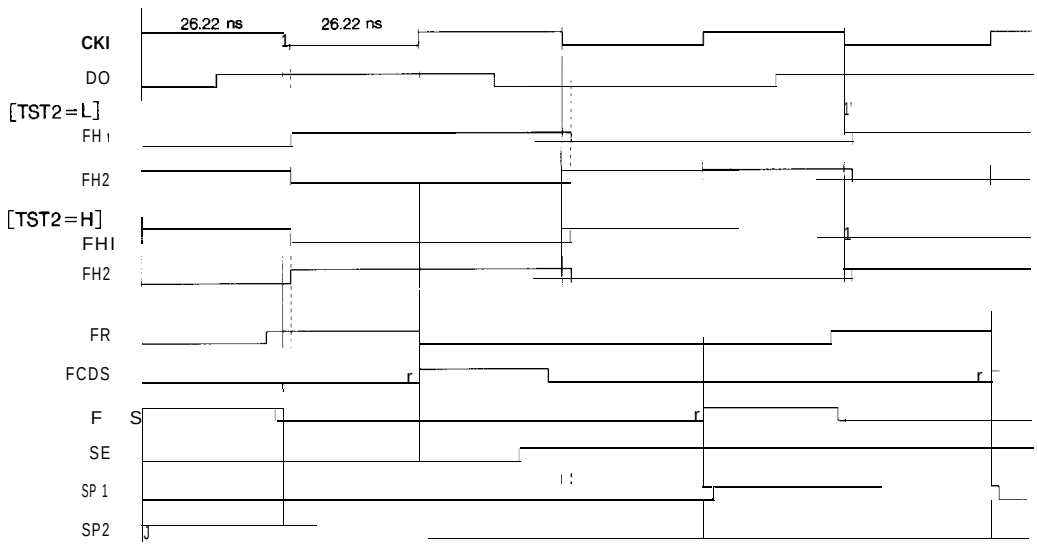
(1st, 3rd FIELD)



(2nd, 4th FIELD)



HIGH SPEED PULSES TIMING



※MFS_1 = MFS2 = MCD_1 = MCD_2 = MFR1 = MFR2= L, SESL = H